FIG. 1

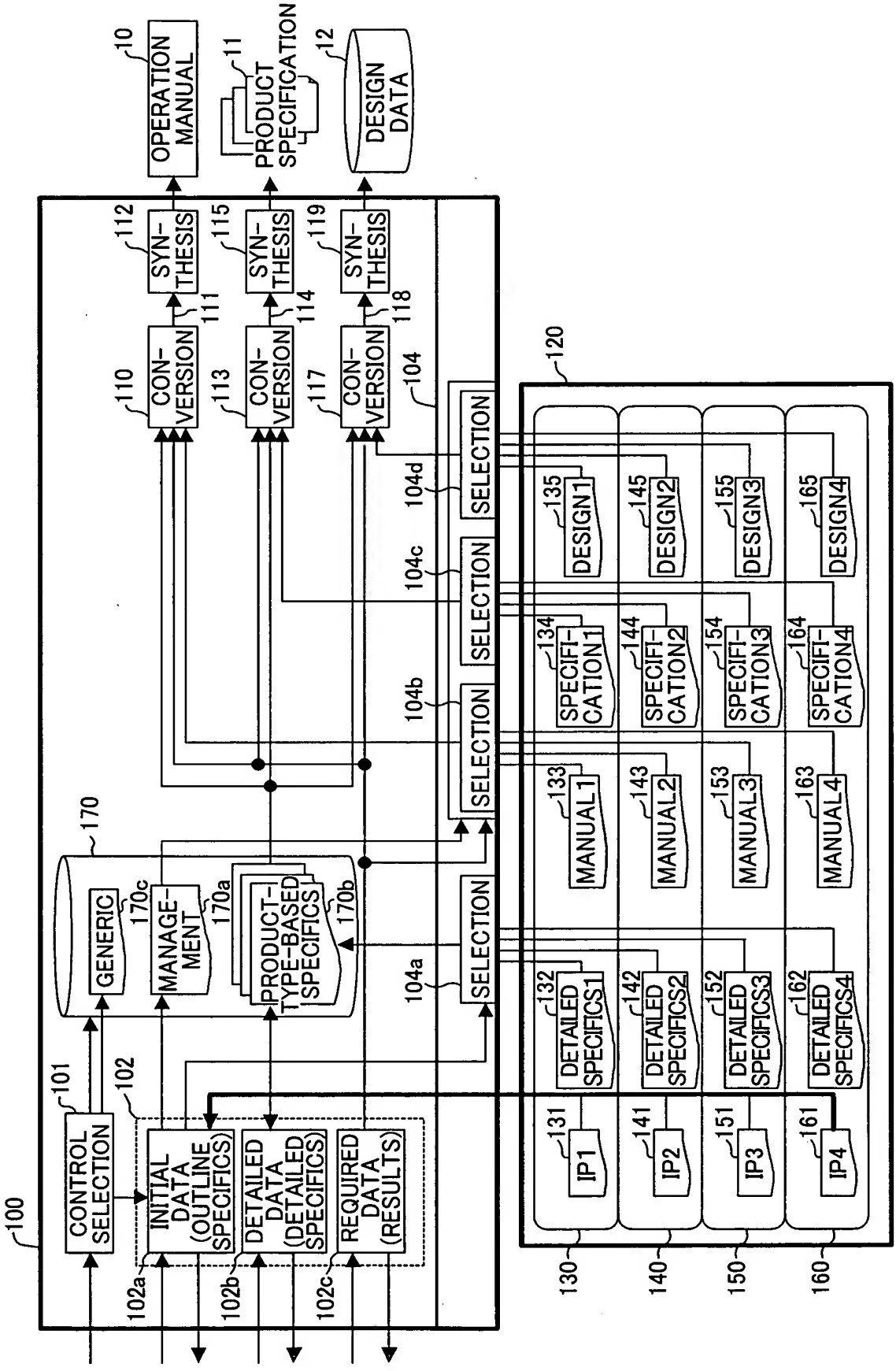

100
CONTROL SELECTION
101
102
INITIAL DATA (OUTLINE SPECIFICS)
DETAILED DATA (DETAILED SPECIFICS)
REQUIRED DATA (RESULTS)
102a
102b
102c
170
GENERIC
170c
MANAGE-MENT
170a
PRODUCT-TYPE-BASED SPECIFICS
170b
110
CON-VERSION
111
SYN-THESIS
112
113
CON-VERSION
114
SYN-THESIS
115
117
CON-VERSION
118
SYN-THESIS
119
10
OPERATION MANUAL
11
PRODUCT SPECIFICATION
12
DESIGN DATA
104
104a
104b
104c
104d
SELECTION
120
130
140
150
160
131
IP1
141
IP2
151
IP3
161
IP4
132
DETAILED SPECIFICS1
142
DETAILED SPECIFICS2
152
DETAILED SPECIFICS3
162
DETAILED SPECIFICS4
133
MANUAL1
143
MANUAL2
153
MANUAL3
163
MANUAL4
134
SPECIFI-CATION1
144
SPECIFI-CATION2
154
SPECIFI-CATION3
164
SPECIFI-CATION4
135
DESIGN1
145
DESIGN2
155
DESIGN3
165
DESIGN4

FIG. 2

131

IP1 = J710M0_PORT
INSTANCE = XXXX
a:DETAILED SPECIFICS 1
b:MANUAL 1
c:SPECIFICATION 1
d:DESIGN 1

FIG. 3

132

PORTn	PnOUT	PnIN	PnDIR	PnPLU
	ADDRESS	ADDRESS	ADDRESS	ADDRESS
	MSB...LSB	MSB...LSB	MSB...LSB	MSB...LSB
0				
1				

FIG. 4

133

REGISTER NAME	DESCRIPTIONS (WITH PnDIR)	DESCRIPTIONS (WITHOUT PnDIR)
PnOUT	TO OUTPUT DATA TO A TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (PnDIR) FOR THE PORT n TO 1 AND WRITE THE DATA ON THE OUTPUT REGISTER (PnOUT) FOR THE PORT n.	TO OUTPUT DATA TO A TERMINAL, WRITE THE DATA ON THE OUTPUT REGISTER (PnOUT) FOR THE PORT n.
PnIN	TO READ THE DATA INPUTTED TO THE TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (PnDIR) FOR THE PORT n TO 0 AND READ OUT THE VALUE OF THE INPUT REGISTER (PnIN) FOR THE PORT n.	TO READ THE DATA INPUTTED TO THE TERMINAL, READ OUT THE VALUE OF THE INPUT REGISTER (PnIN) FOR THE PORT n.
PnDIR	IN THE PORT n, INPUT/OUTPUT DIRECTIONS CAN BE CONTROLLED ON A BIT-BY-BIT BASIS BY THE DIRECTION CONTROL REGISTER (PnDIR) FOR THE PORT n. WHEN THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (PnDIR) FOR THE PORT n INDICATES 1, AN OUTPUT MODE RESULTS, AND WHEN THE CONTROL FLAG INDICATES 0, AN INPUT MODE RESULTS.	–
PnPLU	IN THE PORT n, PRESENCE OR ABSENCE OF A PULL-UP RESISTOR CAN BE SELECTED ON A BIT-BY-BIT BASIS BY THE PULL-UP RESISTOR CONTROL REGISTER (PnPLU) FOR THE PORT n. WHEN THE CONTROL FLAG OF THE PULL-UP RESISTOR CONTROL REGISTER (PnPLU) OF THE PORT n IS SET TO 1, A PULL-UP RESISTOR IS ADDED.	=

FIG. 5

134

Pnm

INPUT VOLTAGE HIGH LEVEL	V_{IH}		$0.8V_{DD}$		V_{DD}	V
INPUT VOLTAGE LOW LEVEL	V_{IL}		V_{SS}		$0.2V_{DD}$	
PULL-UP RESISTOR	R_{IH}	WITH PULL-UP RESISTOR V_{IN} =1.2 V	36	90	180	kΩ
INPUT LEAKAGE CURRENT	I_{LI}	WITHOUT PULL-UP RESISTOR V_{IN} =0~V_{DD}			±2	μA
OUTPUT VOLTAGE HIGH LEVEL	V_{OH}	I_{OH}=−300 μA	2.4			V
OUTPUT VOLTAGE LOW LEVEL	V_{OL}	I_{OL}= 1.6 mA			0.6	

FIG. 6

135

MODULE FROM WHICH WIRING STARTS			MODULE TO WHICH WIRING EXTENDS		
MODULE	INSTANCE	TERMINAL	MODULE	INSTANCE	TERMINAL
J710M0_PORT		p0out0			
			J710M0_PORT		p0in0
J710M0_PORT		p0dir0			
J710M0_PORT		p0plu0			
≈			≈		≈
J710M0_PORT		p1out7			
			J710M0_PORT		p1in7
J710M0_PORT		p1dir7			
J710M0_PORT		p1plu7			

FIG. 7

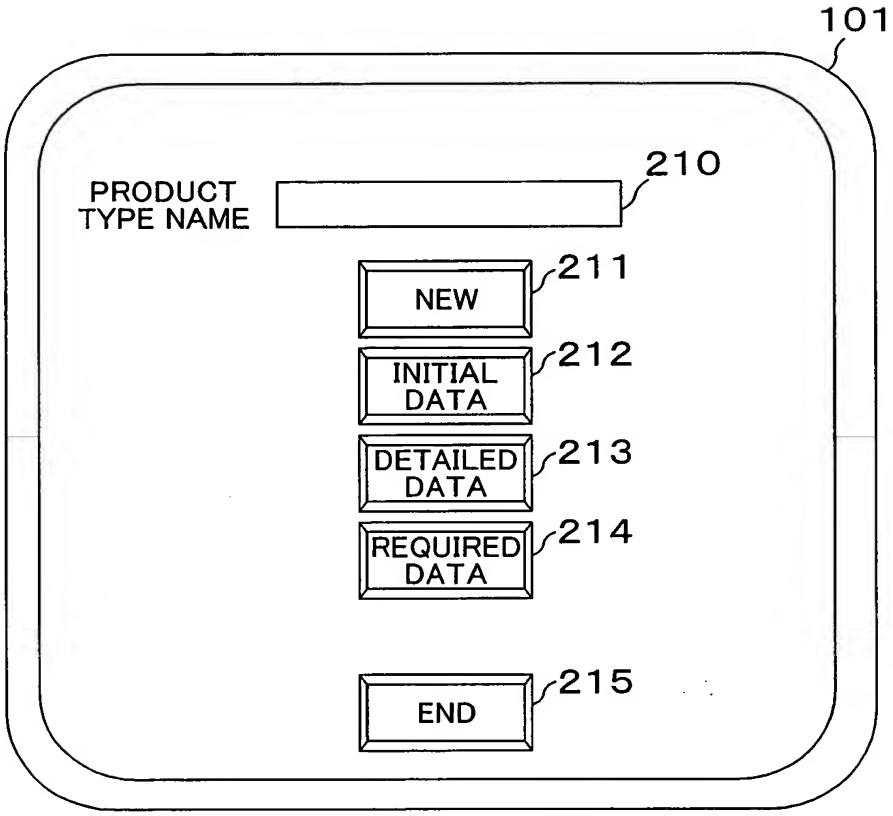

101
210
PRODUCT TYPE NAME
211
NEW
212
INITIAL DATA
213
DETAILED DATA
214
REQUIRED DATA
215
END

FIG. 8

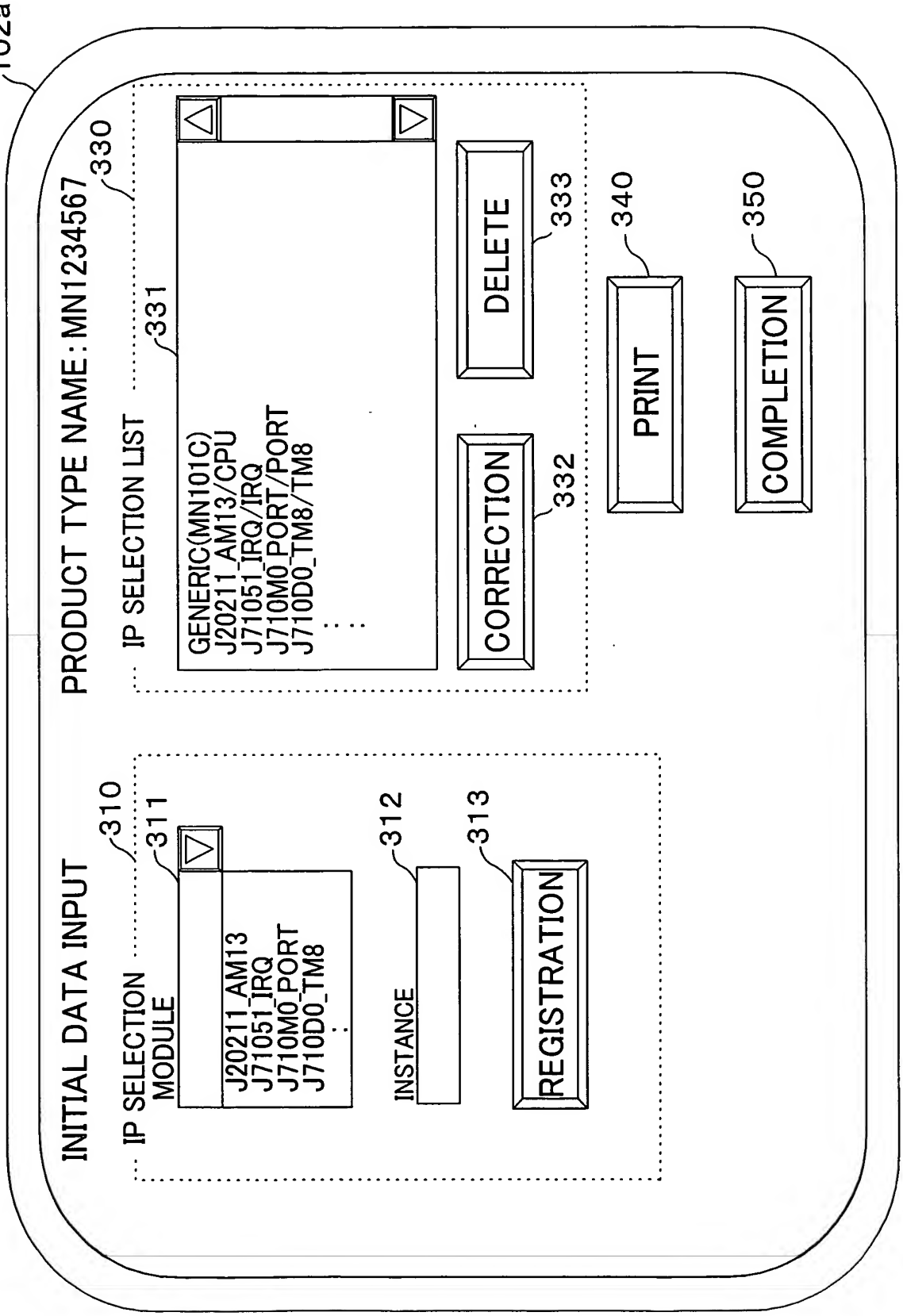

102a
INITIAL DATA INPUT
310
IP SELECTION MODULE
311
J20211_AM13
J71051_IRQ
J710M0_PORT
J710D0_TM8
312
INSTANCE
313
REGISTRATION
PRODUCT TYPE NAME: MN1234567
330
IP SELECTION LIST
331
GENERIC(MN101C)
J20211_AM13/CPU
J71051_IRQ/IRQ
J710M0_PORT/PORT
J710D0_TM8/TM8
CORRECTION
332
DELETE
333
PRINT
340
COMPLETION
350

FIG. 9

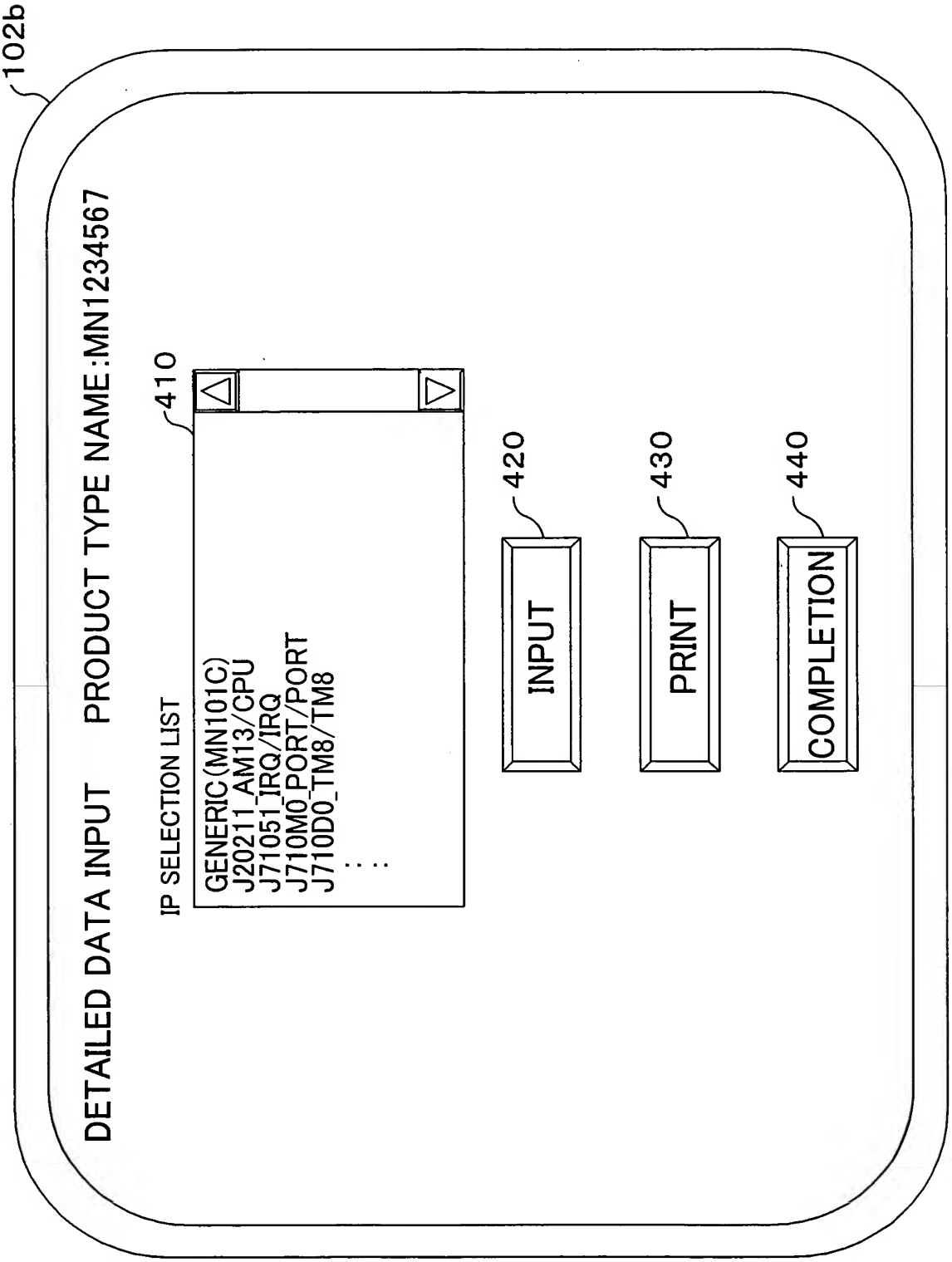

102b
DETAILED DATA INPUT PRODUCT TYPE NAME:MN1234567
IP SELECTION LIST
410
GENERIC(MN101C)
J20211_AM13/CPU
J71051_IRQ/IRQ
J710M0_PORT/PORT
J710D0_TM8/TM8
. . .
420
INPUT
430
PRINT
440
COMPLETION

FIG. 10

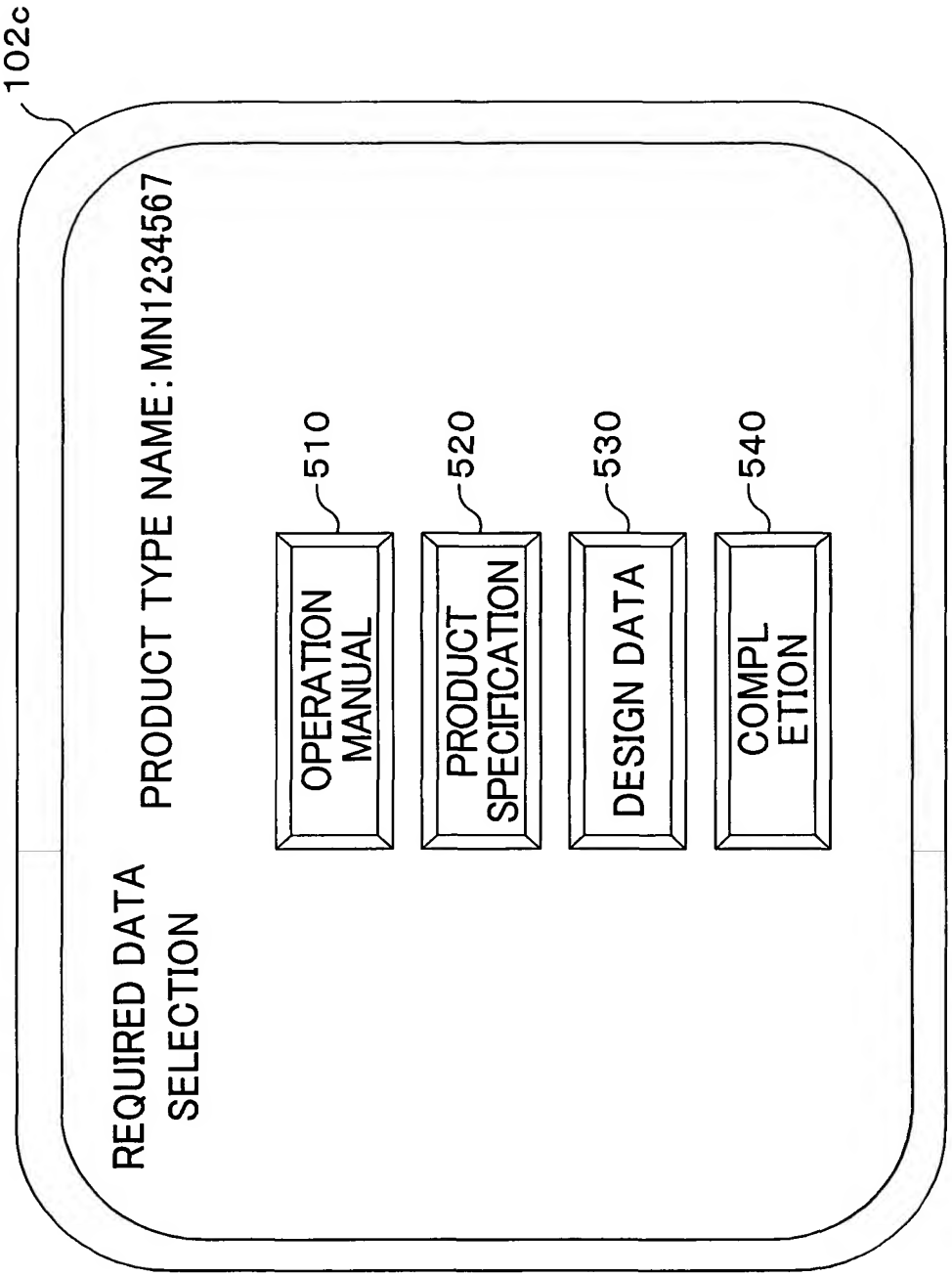

102c
PRODUCT TYPE NAME : MN1234567
REQUIRED DATA SELECTION
510
OPERATION MANUAL
520
PRODUCT SPECIFICATION
530
DESIGN DATA
540
COMPL ETION

FIG. 11

170a

```
IP2=J20211_AM13
  INSTANCE=        CPU
  a:DETAILED SPECIFICS 2
  b:MANUAL 2
  c:SPECIFICATION 2
  d:DESIGN2

IP3=J71051_IRQ
  INSTANCE=IRQ
  a:DETAILED SPECIFICS3
  b:MANUAL3
  c:SPECIFICATION 3
  d:DESIGN3

IP1=J710M0_PORT
  INSTANCE=PORT
  a:DETAILED SPECIFICS1
  b:MANUAL1
  c:SPECIFICATION 1
  d:DESIGN1

IP4=J710D0_TM8
  INSTANCE=TM8
  a:DETAILED SPECIFICS4
  b:MANUAL4
  c:SPECIFICATION 4
  d:DESIGN4
```

FIG. 12

170b

PORTn	PnOUT	PnIN	PnDIR	PnPLU
	ADDRESS	ADDRESS	ADDRESS	ADDRESS
	MSB...LSB	MSB...LSB	MSB...LSB	MSB...LSB
0	3F10	3F20	3F30	3F40
	01111111	01111111	01111111	01111111
1	3F11	3F21	NOT	3F41
	00011111	00011111		00011111

FIG. 13

111

```
<section><heading>DESCRIPTIONS FOR PORT 0</heading>
<section position ="square">
<heading>SETTING OF GENERAL-PURPOSE PORT</heading>
<para>TO OUTPUT DATA TO A TERMINAL, SET THE CONTROL FLAG OF
THE DIRECTION CONTROL REGISTER (PODIR) FOR THE PORT 0 TO 1
AND WRITE THE DATA ON THE OUTPUT REGISTER (POOUT) FOR THE
PORT 0.</para>
<para>TO READ THE DATA INPUTTED TO THE TERMINAL, SET THE
CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (PODIR) FOR THE
PORT 0 TO 0 AND READ OUT THE VALUE OF THE INPUT REGISTER
(POIN) FOR THE PORT 0.</para>
<para>IN THE PORT 0, INPUT/OUTPUT DIRECTIONS CAN BE CONTROLLED ON A
BIT-BY-BIT BASIS BY THE DIRECTION CONTROL REGISTER (PODIR) FOR THE
PORT 0.  WHEN THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER
(PODIR) FOR THE PORT 0 INDICATES 1, AN OUTPUT MODE RESULTS, AND
WHEN THE CONTROL FLAG INDICATES 0, AN INPUT MODE RESULTS.</para>
<para>IN THE PORT 0, PRESENCE OR ABSENCE OF A PULL-UP RESISTOR CAN
BE SELECTED ON A BIT-BY-BIT BASIS BY THE PULL-UP RESISTOR CONTROL
REGISTER (POPLU) FOR THE PORT 0.  WHEN THE CONTROL FLAG OF THE
PULL-UP RESISTOR CONTROL REGISTER (POPLU) OF THE PORT 0 IS SET TO
1, A PULL-UP RESISTOR IS ADDED.</para>
</section> </section>
<section><heading>DESCRIPTIONS FOR PORT 1</heading>
<section position ="square">
<heading>SETTING OF GENERAL-PURPOSE PORT</heading>
<para>TO OUTPUT DATA TO A TERMINAL, WRITE THE DATA ON THE OUTPUT
REGISTER (P1OUT) FOR THE PORT 1.</para>
<para>TO READ THE DATA INPUTTED TO THE TERMINAL, READ OUT THE VALUE
OF THE INPUT REGISTER (P1IN) FOR THE PORT 1.</para>
<para>IN THE PORT 1, PRESENCE OR ABSENCE OF A PULL-UP RESISTOR CAN
BE SELECTED ON A BIT-BY-BIT BASIS BY THE PULL-UP RESISTOR CONTROL
REGISTER (P1PLU) FOR THE PORT 1.  WHEN THE CONTROL FLAG OF THE
PULL-UP RESISTOR CONTROL REGISTER (P1PLU) OF THE PORT 1 IS SET TO
1, A PULL-UP RESISTOR IS ADDED.</para>
</section></section>
```

FIG. 14

114

P00

INPUT VOLTAGE HIGH LEVEL	V_{IH}		$0.8V_{DD}$		V_{DD}	V
INPUT VOLTAGE LOW LEVEL	V_{IL}		V_{SS}		$0.2V_{DD}$	
PULL-UP RESISTOR	R_{IH}	WITH PULL-UP RESISTOR V_{IN} =1.2 V	36	90	180	kΩ
INPUT LEAKAGE CURRENT	I_{LI}	WITHOUT PULL-UP RESISTOR V_{IN} =0~V_{DD}			±2	μA
OUTPUT VOLTAGE HIGH LEVEL	V_{OH}	I_{OH}=−300 μA	2.4			V
OUTPUT VOLTAGE LOW LEVEL	V_{OL}	I_{OL}= 1.6 mA			0.6	

P01

INPUT VOLTAGE HIGH LEVEL	V_{IH}		$0.8V_{DD}$		V_{DD}	V
INPUT VOLTAGE LOW LEVEL	V_{IL}		V_{SS}		$0.2V_{DD}$	
PULL-UP RESISTOR	R_{IH}	WITH PULL-UP RESISTOR V_{IN} =1.2 V	36	90	180	kΩ
INPUT LEAKAGE CURRENT	I_{LI}	WITHOUT PULL-UP RESISTOR V_{IN} =0~V_{DD}			±2	μA
OUTPUT VOLTAGE HIGH LEVEL	V_{OH}	I_{OH}=−300 μA	2.4			V
OUTPUT VOLTAGE LOW LEVEL	V_{OL}	I_{OL}= 1.6 mA			0.6	

FIG. 15

118

MODULE FROM WHICH WIRING STARTS			MODULE TO WHICH WIRING EXTENDS		
MODULE	INSTANCE	TERMINAL	MODULE	INSTANCE	TERMINAL
J710M0_PORT	PORT	p0out0	iobuf	p00io	out
iobuf	p00io	in	J710M0_PORT	PORT	p0in0
J710M0_PORT	PORT	p0dir0	iobuf	p00io	dir
J710M0_PORT	PORT	p0plu0	iobuf	p00io	plu
≈			≈		≈
J710M0_PORT	PORT	p1out7	open	open	open
iobuf	FIX	0	J710M0_PORT	PORT	p1in7
J710M0_PORT	PORT	p1dir7	open	open	open
J710M0_PORT	PORT	p1plu7	open	open	open

FIG. 16

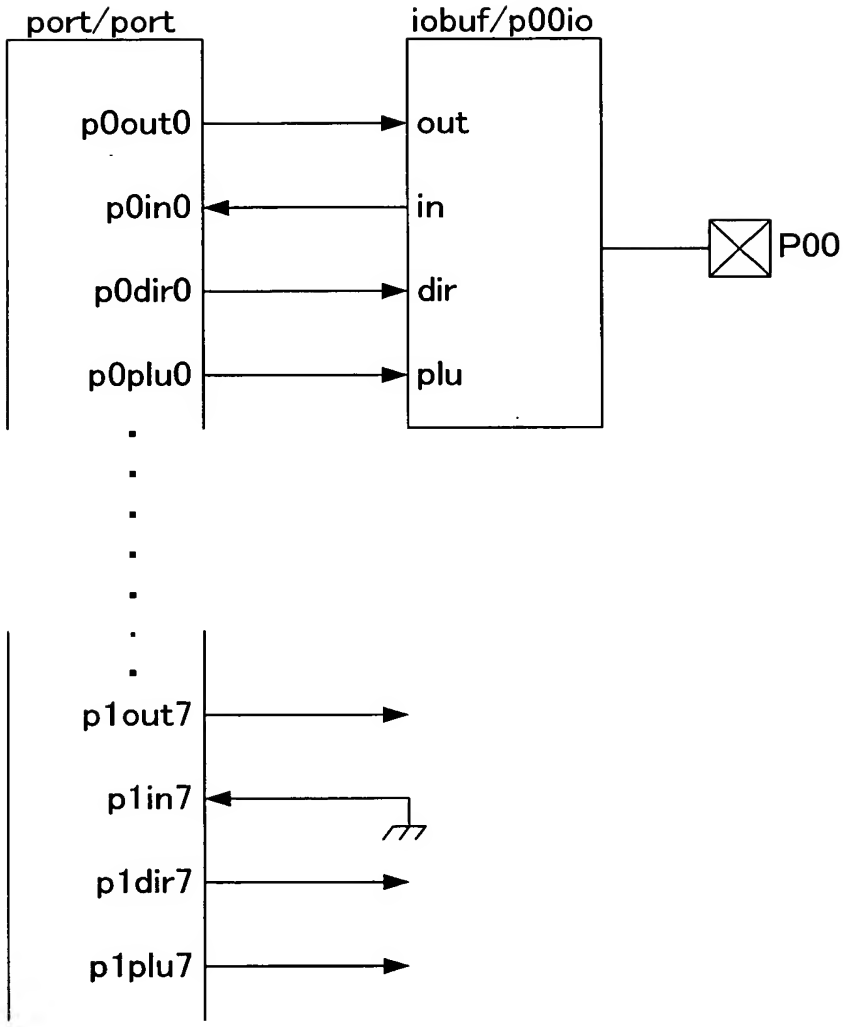

port/port
iobuf/p00io
p0out0
out
p0in0
in
P00
p0dir0
dir
p0plu0
plu
p1out7
p1in7
p1dir7
p1plu7

FIG. 17

10

4.1 FUNCTIONS OF PORT 0

4.1.1 DESCRIPTIONS FOR PORT 0

■SETTING OF GENERAL-PURPOSE PORT

TO OUTPUT DATA TO A TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P0DIR) FOR THE PORT 0 TO 1 AND WRITE THE DATA ON THE OUTPUT REGISTER (P0OUT) FOR THE PORT 0.

TO READ THE DATA INPUTTED TO THE TERMINAL, SET THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P0DIR) FOR THE PORT 0 TO 0 AND READ OUT THE VALUE OF THE INPUT REGISTER (P0IN) FOR THE PORT 0.

IN THE PORT 0, INPUT/OUTPUT DIRECTIONS CAN BE CONTROLLED ON A BIT-BY-BIT BASIS BY THE DIRECTION CONTROL REGISTER (P0DIR) FOR THE PORT 0. WHEN THE CONTROL FLAG OF THE DIRECTION CONTROL REGISTER (P0DIR) FOR THE PORT 0 INDICATES 1, AN OUTPUT MODE RESULTS, AND WHEN THE CONTROL FLAG INDICATES 0, AN INPUT MODE RESULTS.

IN THE PORT 0, PRESENCE OR ABSENCE OF A PULL-UP RESISTOR CAN BE SELECTED ON A BIT-BY-BIT BASIS BY THE PULL-UP RESISTOR CONTROL REGISTER (P0PLU) FOR THE PORT 0. WHEN THE CONTROL FLAG OF THE PULL-UP RESISTOR CONTROL REGISTER (P0PLU) OF THE PORT 0 IS SET TO 1, A PULL-UP RESISTOR IS ADDED.

FIG. 18

11

	PRODUCT SPECIFICATION	MN1234567			
		ALL PAGES IN SPECIFICATION	-	PAGE	10

C. ELECTRIC CHARACTERISTICS Ta=-40°C～+85°C V_{DD}=3 V V_{SS}=0 V

ITEM	ABBREVIATION	CONDITION	ALLOWABLE VALUE			UNIT
			MIN-IMUM	STAND-ARD	MAX-IMUM	
P00						
INPUT VOLTAGE HIGH LEVEL	V_{IH}		$0.8V_{DD}$		V_{DD}	V
INPUT VOLTAGE LOW LEVEL	V_{IL}		V_{SS}		$0.2V_{DD}$	V
PULL-UP RESISTOR	R_{IH}	WITH PULL-UP RESISTOR V_{IN} =1.2 V	36	90	180	kΩ
INPUT LEAKAGE CURRENT	I_{LI}	WITHOUT PULL-UP RESISTOR V_{IN} =0～V_{DD}			±2	μA
OUTPUT VOLTAGE HIGH LEVEL	V_{OH}	I_{OH}=−300 μA	2.4			V
OUTPUT VOLTAGE LOW LEVEL	V_{OL}	I_{OL}= 1.6 mA			0.6	V

FIG. 19

12

```
module SAMPLE (
P00,
:
:
P17);

input    P00;
:
:
input    P17;

wire     p00io_in_net0;
:
:
wire     p17io_in_net7;
wire     PORT_p0dir0_net8;
wire     PORT_p0out0_net9;
wire     PORT_p0plu0_net10;
:
:
wire     PORT_p1dir7_net53;
wire     PORT_p1out7_net54;
wire     PORT_p1plu7_net55;

iobuf p00io (
.io(P00),
.in(p00io_in_net0),
.dir(PORT_p0dir0_net8),
.out(PORT_p0out0_net9),
.plu(PORT_p0plu0_net10));
:
:
```

FIG. 20

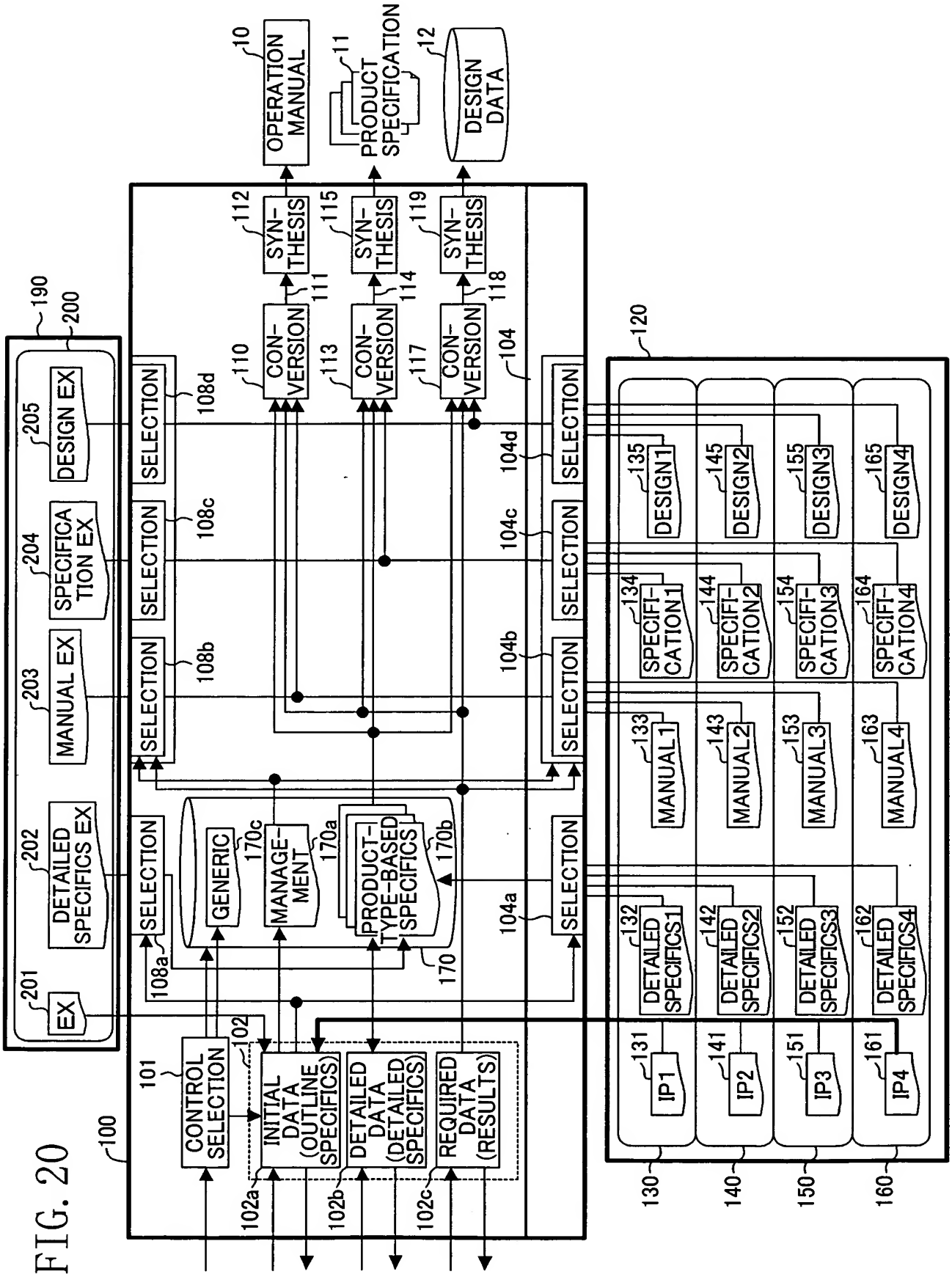

100
101
CONTROL SELECTION
102
INITIAL DATA (OUTLINE SPECIFICS)
DETAILED DATA (DETAILED SPECIFICS)
REQUIRED DATA (RESULTS)
102a
102b
102c
190
200
201
EX
202
DETAILED SPECIFICS EX
203
MANUAL EX
204
SPECIFICATION EX
205
DESIGN EX
108a
SELECTION
GENERIC
170c
MANAGEMENT
170a
PRODUCT-TYPE-BASED SPECIFICS
170b
170
108b
108c
108d
104a
104b
104c
104d
110
CONVERSION
111
SYNTHESIS
112
113
114
115
117
118
119
104
10
OPERATION MANUAL
11
PRODUCT SPECIFICATION
12
DESIGN DATA
120
130
140
150
160
131
IP1
141
IP2
151
IP3
161
IP4
132
DETAILED SPECIFICS1
142
DETAILED SPECIFICS2
152
DETAILED SPECIFICS3
162
DETAILED SPECIFICS4
133
MANUAL1
143
MANUAL2
153
MANUAL3
163
MANUAL4
134
SPECIFICATION1
144
SPECIFICATION2
154
SPECIFICATION3
164
SPECIFICATION4
135
DESIGN1
145
DESIGN2
155
DESIGN3
165
DESIGN4

FIG. 21

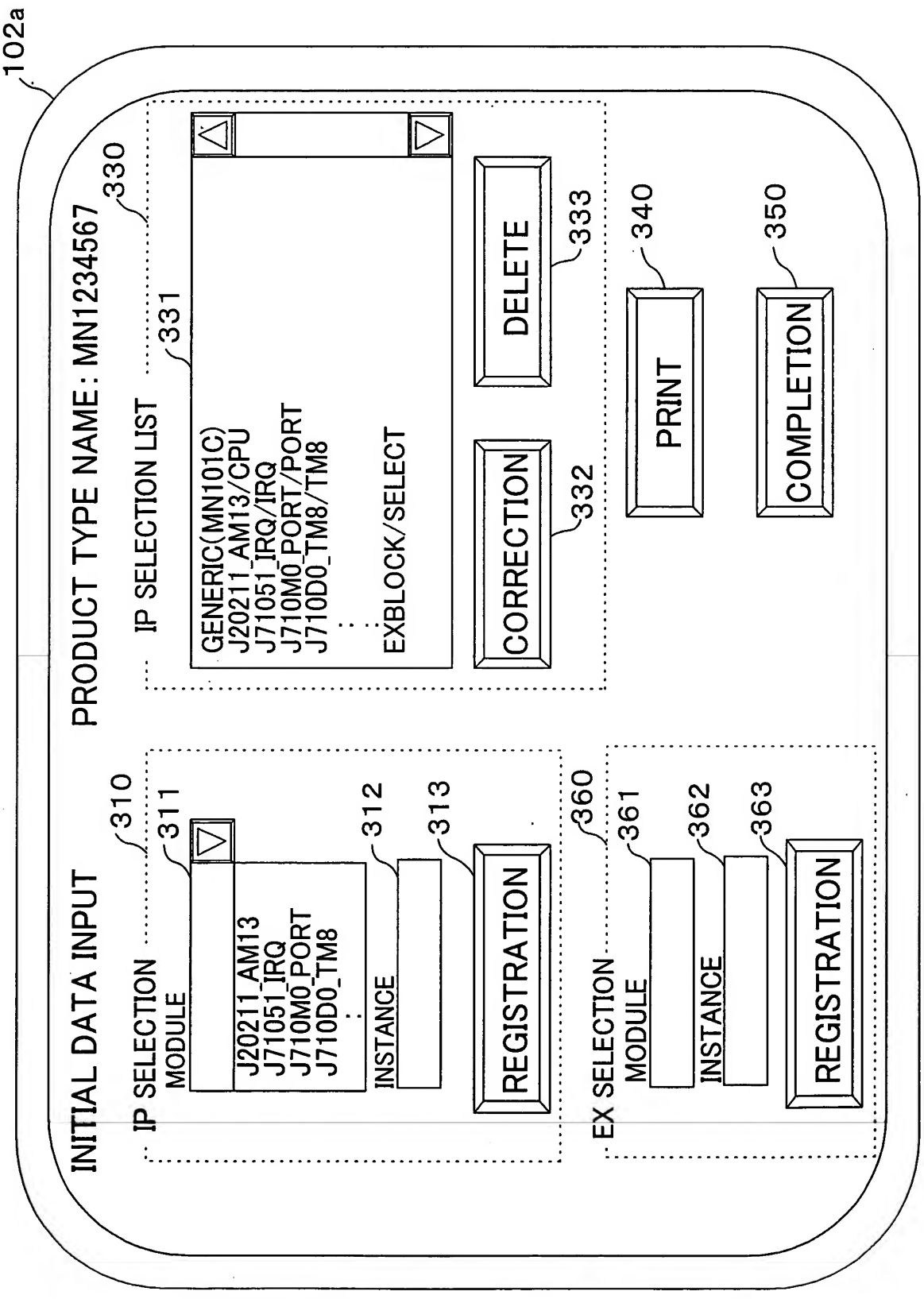

102a
INITIAL DATA INPUT
PRODUCT TYPE NAME: MN1234567
330
IP SELECTION LIST
331
GENERIC(MN101C)
J20211_AM13/CPU
J71051_IRQ/IRQ
J710M0_PORT/PORT
J710D0_TM8/TM8
EXBLOCK/SELECT
DELETE
333
CORRECTION
332
PRINT
340
COMPLETION
350
310
IP SELECTION
MODULE
311
J20211_AM13
J71051_IRQ
J710M0_PORT
J710D0_TM8
312
INSTANCE
313
REGISTRATION
360
EX SELECTION
MODULE
361
362
INSTANCE
363
REGISTRATION

FIG. 22

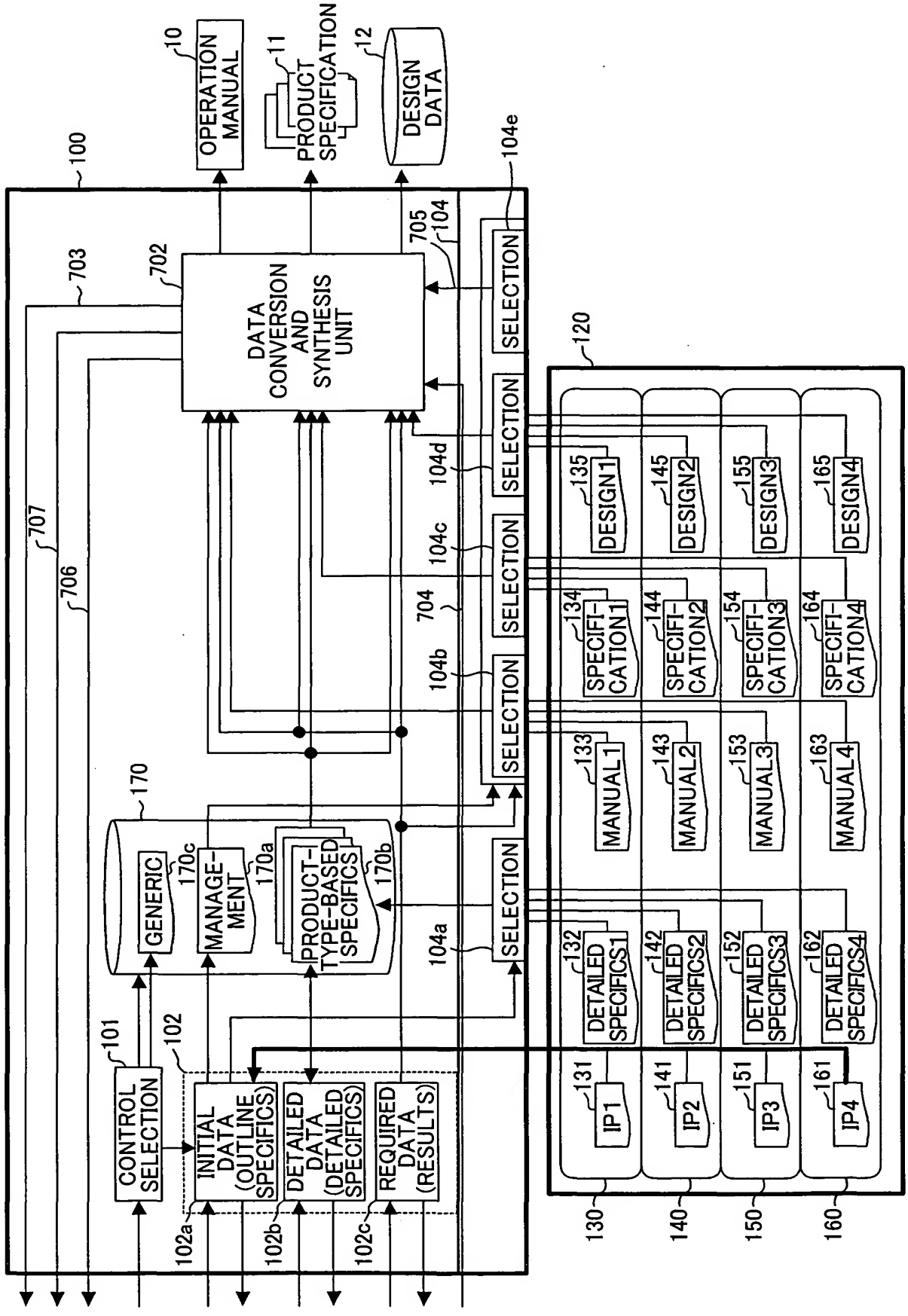

100
OPERATION MANUAL
10
PRODUCT SPECIFICATION
11
DESIGN DATA
12
DATA CONVERSION AND SYNTHESIS UNIT
702
703
705
104
104e
SELECTION
120
707
706
704
104d
104c
104b
104a
170
GENERIC
170c
MANAGE-MENT
170a
PRODUCT-TYPE-BASED SPECIFICS
170b
CONTROL SELECTION
101
102
INITIAL DATA (OUTLINE SPECIFICS)
DETAILED DATA (DETAILED SPECIFICS)
REQUIRED DATA (RESULTS)
102a
102b
102c
130
140
150
160
IP1
IP2
IP3
IP4
131
141
151
161
DETAILED SPECIFICS1
DETAILED SPECIFICS2
DETAILED SPECIFICS3
DETAILED SPECIFICS4
132
142
152
162
MANUAL1
MANUAL2
MANUAL3
MANUAL4
133
143
153
163
SPECIFI-CATION1
SPECIFI-CATION2
SPECIFI-CATION3
SPECIFI-CATION4
134
144
154
164
DESIGN1
DESIGN2
DESIGN3
DESIGN4
135
145
155
165

FIG. 23

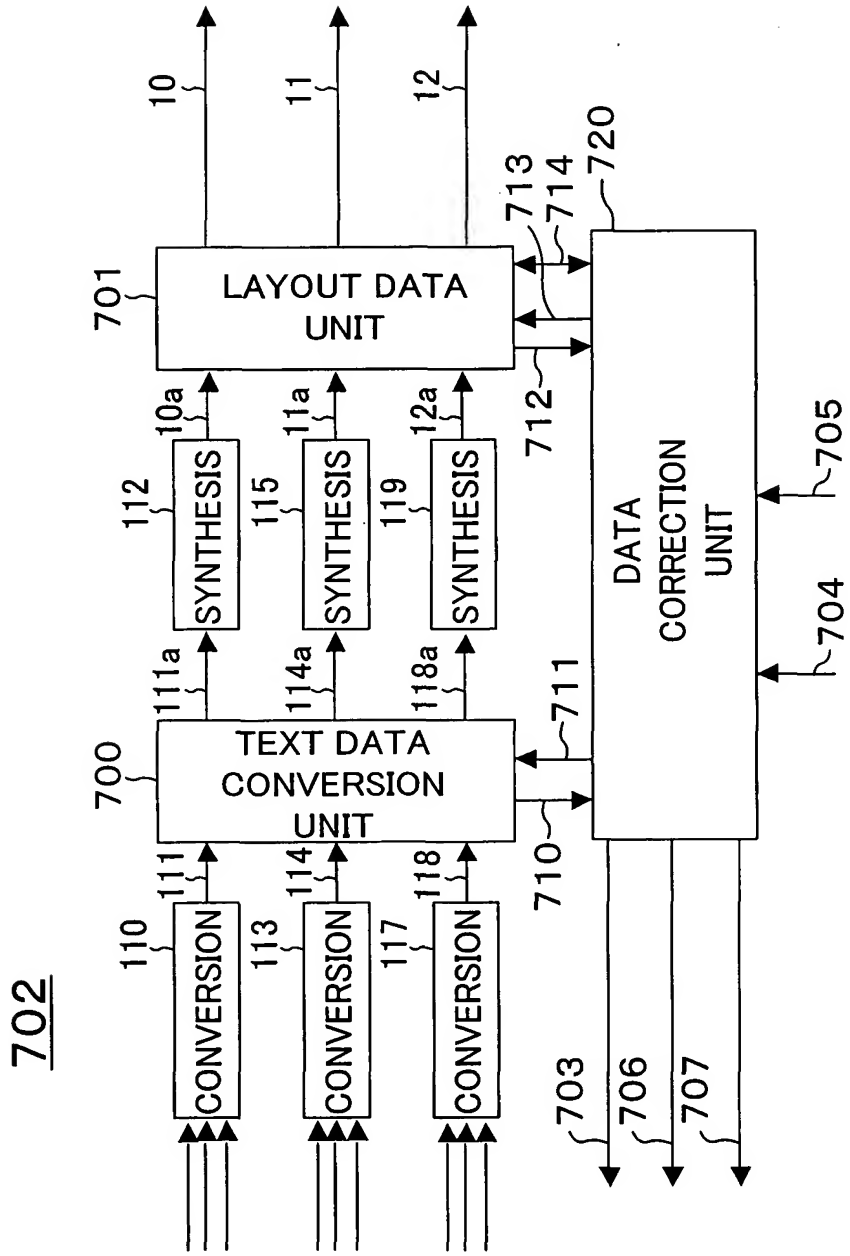

702
CONVERSION
CONVERSION
CONVERSION
TEXT DATA CONVERSION UNIT
SYNTHESIS
SYNTHESIS
SYNTHESIS
LAYOUT DATA UNIT
DATA CORRECTION UNIT
10
11
12
700
701
702
703
704
705
706
707
710
711
712
713
714
720

FIG. 24

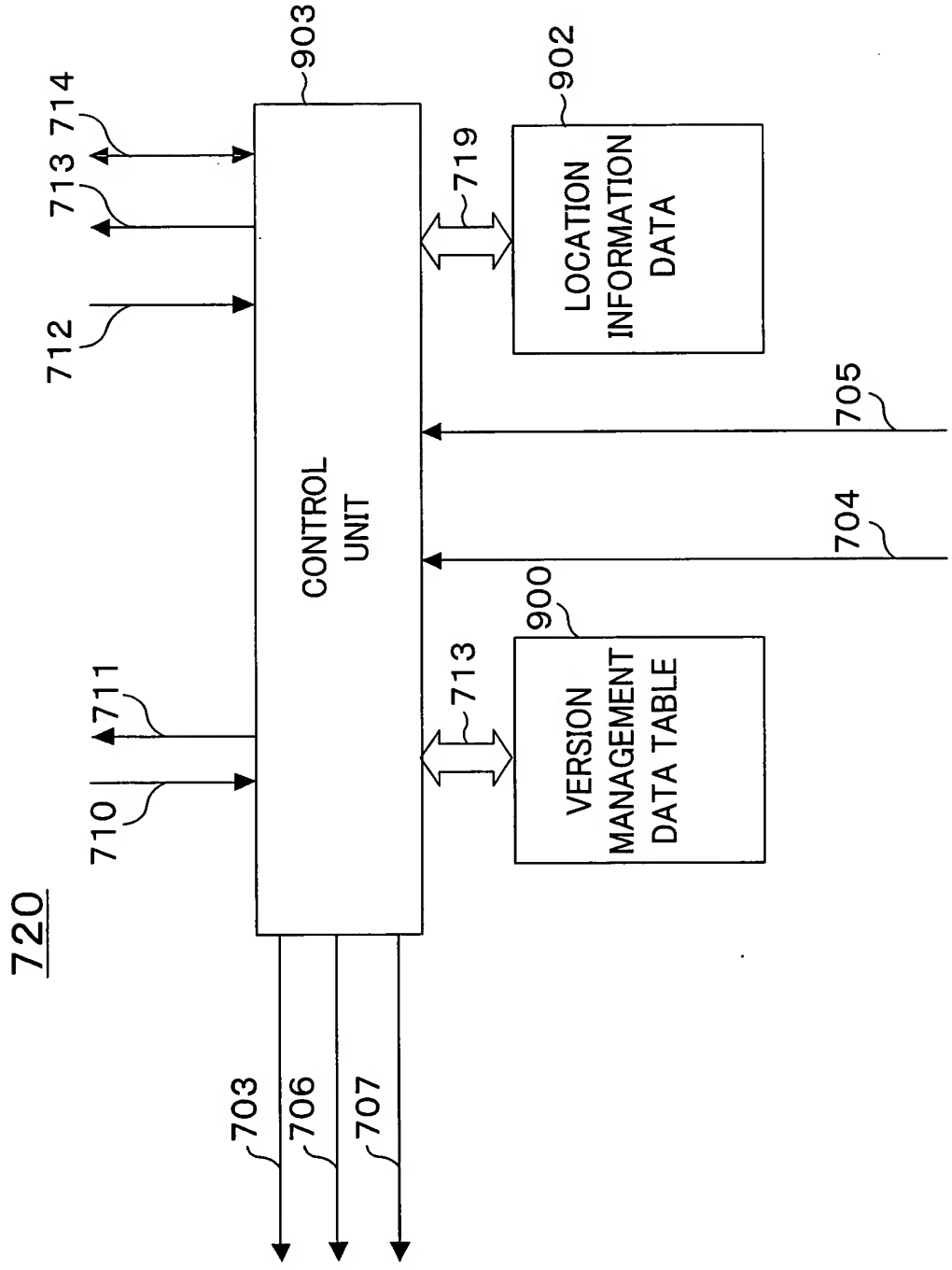

720
CONTROL UNIT
903
902
LOCATION INFORMATION DATA
900
VERSION MANAGEMENT DATA TABLE
710
711
712
713
714
719
703
706
707
704
705

FIG. 25

900

IP MANAGEMENT DATA	VERSION
IP1	Ver 1
IP2	Ver 2
IP3	Ver 2
IP4	Ver 3

FIG. 26

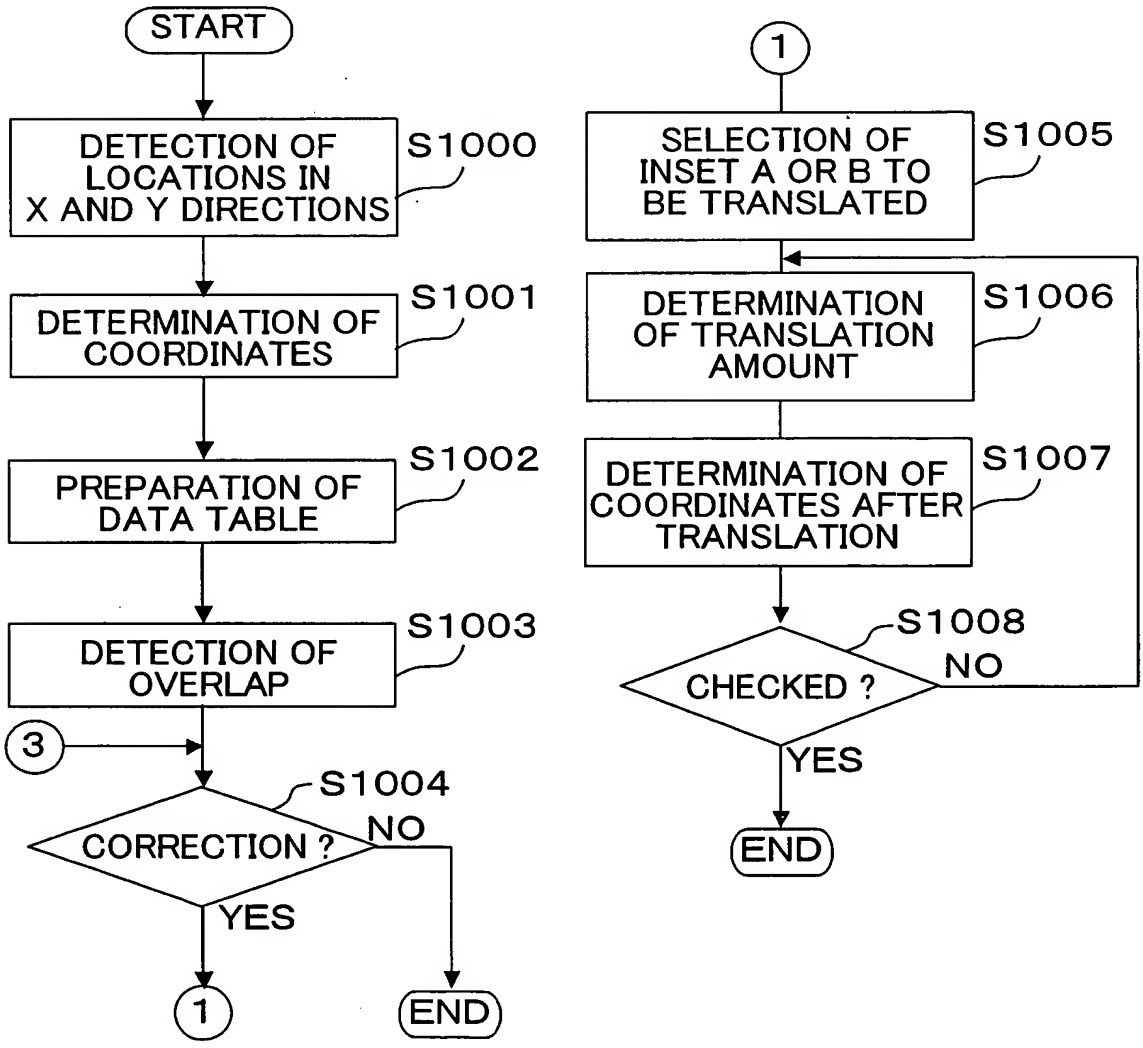


FIG. 27

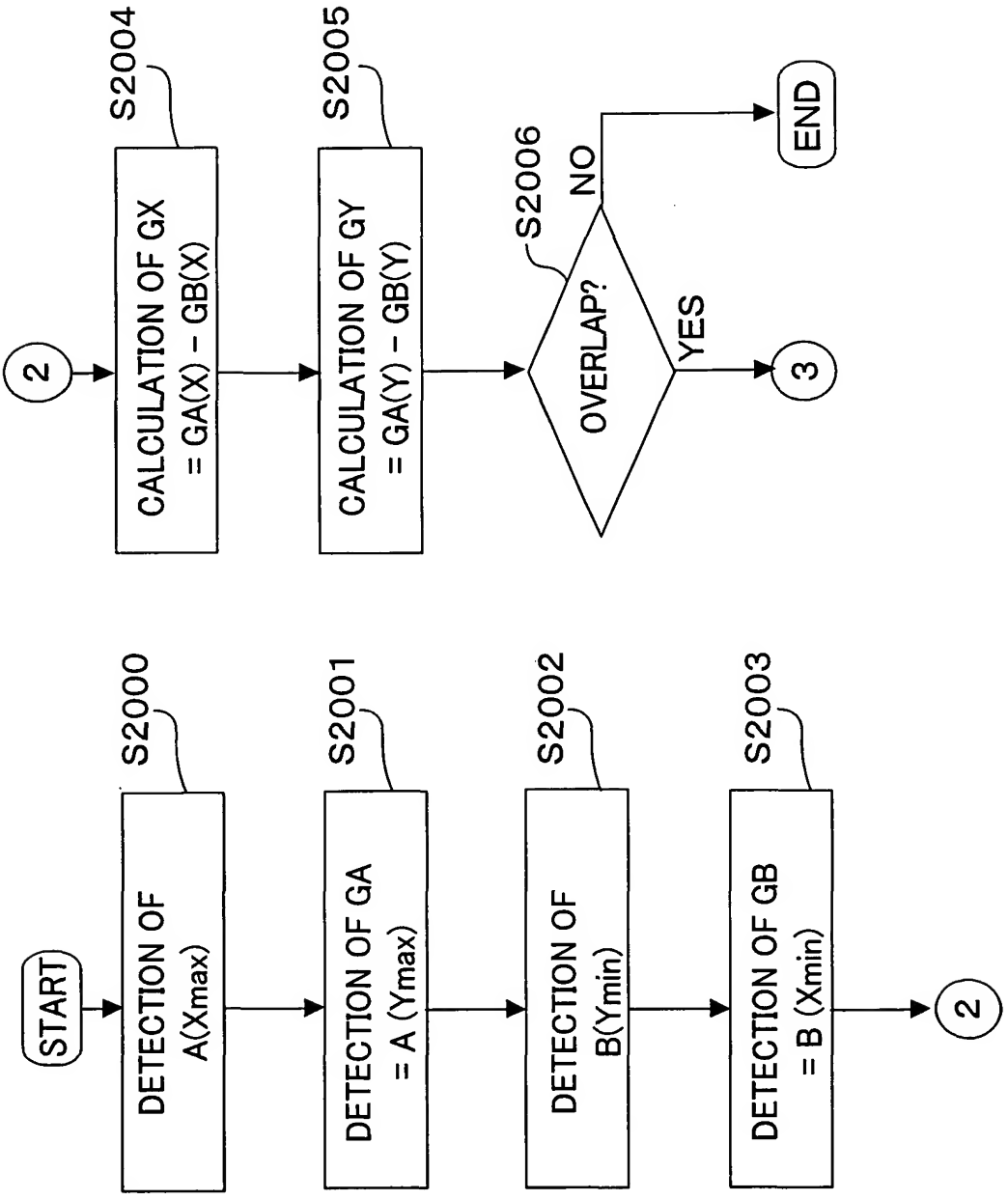

START
S2000
DETECTION OF A(Xmax)
S2001
DETECTION OF GA = A (Ymax)
S2002
DETECTION OF B(Ymin)
S2003
DETECTION OF GB = B (Xmin)
2
2
S2004
CALCULATION OF GX = GA(X) – GB(X)
S2005
CALCULATION OF GY = GA(Y) – GB(Y)
S2006
OVERLAP?
NO
YES
END
3

FIG. 28

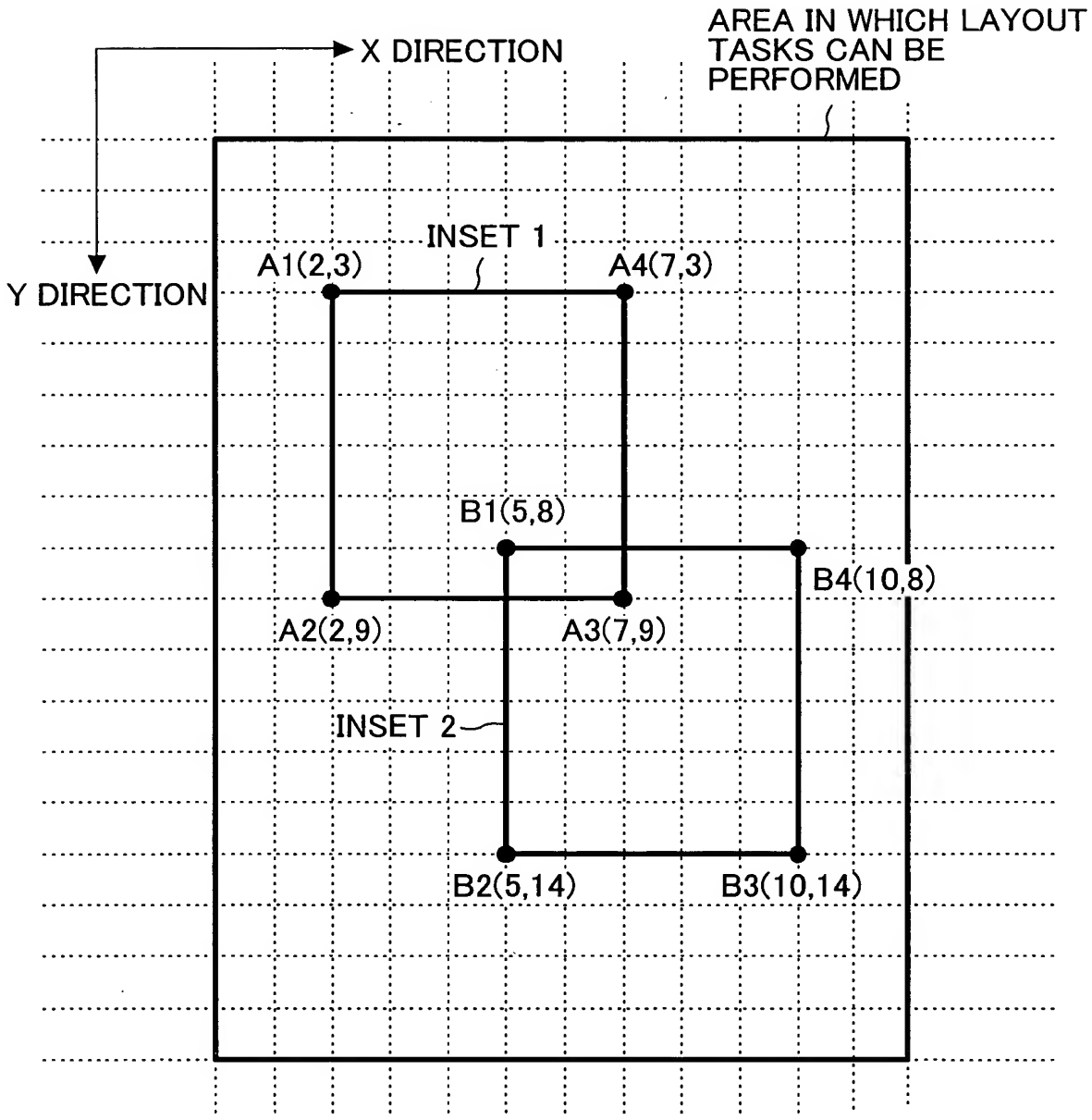

714 BEFORE CORRECTIONS
X DIRECTION
Y DIRECTION
AREA IN WHICH LAYOUT TASKS CAN BE PERFORMED
INSET 1
A1(2,3)
A4(7,3)
B1(5,8)
B4(10,8)
A2(2,9)
A3(7,9)
INSET 2
B2(5,14)
B3(10,14)

FIG. 29

902 BEFORE CORRECTIONS

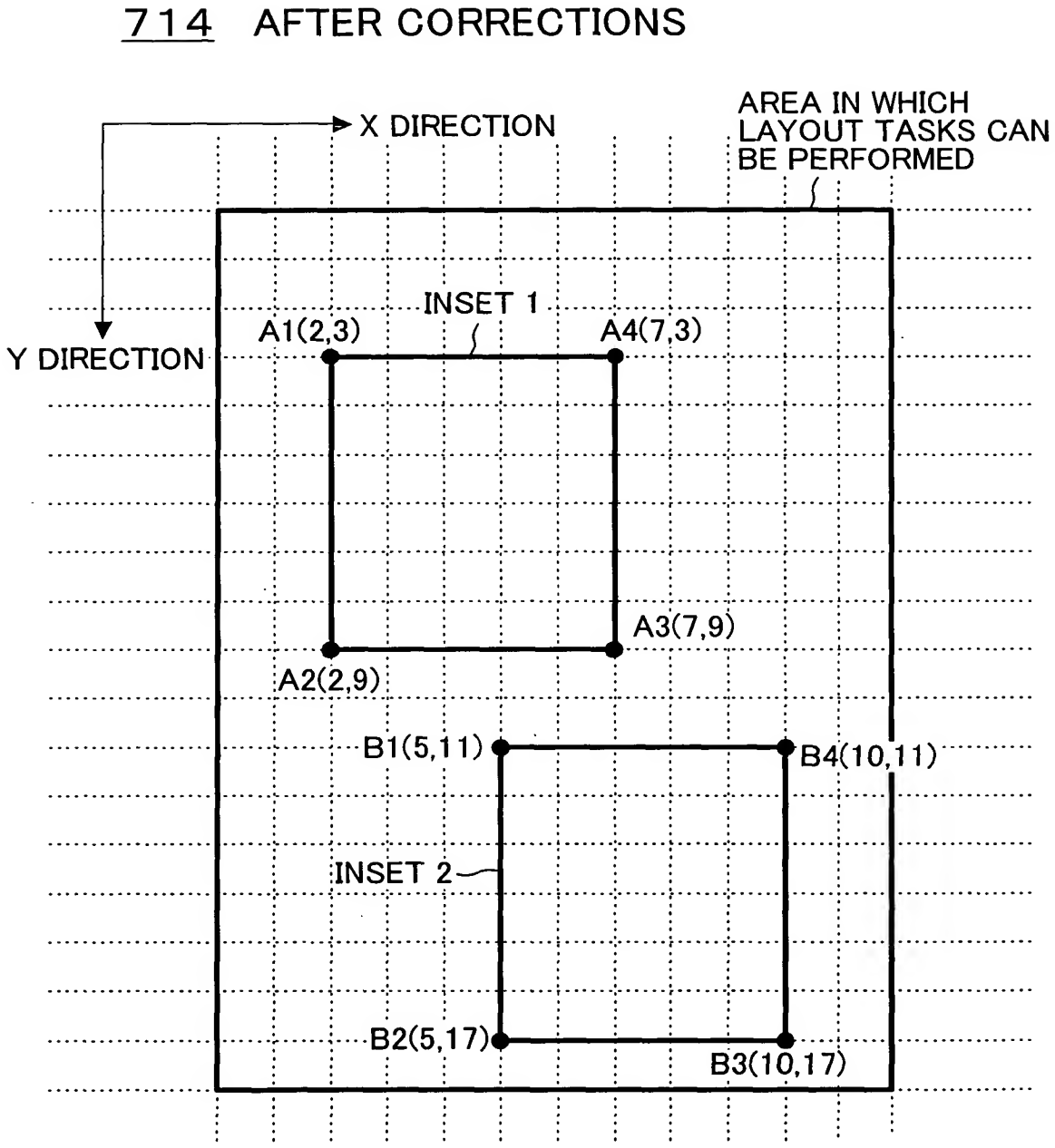
	LOCATION INFOR-MATION1	LOCATION INFOR-MATION2	LOCATION INFOR-MATION3	LOCATION INFOR-MATION4
INSET 1	A1 (2, 3)	A2 (2, 9)	A3 (7, 9)	A4 (7, 3)
INSET 2	B1 (5, 8)	B2 (5, 14)	B3 (10, 14)	B4 (10, 8)

FIG. 30

902 AFTER CORRECTIONS

	LOCATION INFOR-MATION1	LOCATION INFOR-MATION2	LOCATION INFOR-MATION3	LOCATION INFOR-MATION4
INSET 1	A1 (2, 3)	A2 (2, 9)	A3 (7, 9)	A4 (7, 3)
INSET 2	B1 (5, 11)	B2 (5, 17)	B3 (10, 17)	B4 (10, 11)

FIG. 31


714 AFTER CORRECTIONS
X DIRECTION
Y DIRECTION
AREA IN WHICH LAYOUT TASKS CAN BE PERFORMED
INSET 1
A1(2,3)
A4(7,3)
A3(7,9)
A2(2,9)
B1(5,11)
B4(10,11)
INSET 2
B2(5,17)
B3(10,17)